A2

or non-porous inorganic polymers;

implanting silicon ions into said low dielectric constant material layer; and

thereafter depositing a TEOS-based silicon oxide layer overlying said low dielectric constant material whereby there is good adhesion between said low dielectric constant material layer and said TEOS-based silicon oxide layer.

Please cancel Claim 2.

A3

6. (AMENDED) The method according to Claim 1 wherein said TEOS-based silicon oxide layer has a thickness of between about 50 and 5000 Angstroms.

Please cancel Claims 7-11.

A4

12. (AMENDED) A method of dual damascene copper metallization in the fabrication of an integrated circuit device comprising:

depositing a first low dielectric constant material layer over a substrate wherein said first low dielectric constant material comprises: porous or non-porous carbon-based silicon oxides, porous or non-porous doped silicon oxides, porous or non-porous organic polymers, or porous or non-porous inorganic polymers;

implanting silicon ions into said first low dielectric constant material layer;

thereafter depositing a TEOS-based silicon oxide etch stop layer overlying said first low dielectric constant material whereby there is good adhesion between said first low dielectric constant material layer and said TEOS-based silicon oxide etch stop layer;

depositing a second low dielectric constant material layer overlying said etch stop layer wherein said second low dielectric constant material comprises: porous or non-porous carbon-based silicon oxides, porous or non-porous doped silicon oxides, porous or non-porous organic polymers, or porous or non-porous inorganic polymers;

implanting silicon ions into said second low dielectric constant material layer;

thereafter depositing a TEOS-based silicon oxide capping layer overlying said second low dielectric constant material whereby there is good adhesion between said second low dielectric constant material layer and said TEOS-based silicon oxide capping layer;

forming a dual damascene opening through said capping layer, said second low dielectric constant material layer, said etch stop layer, and said first low dielectric constant material layer; and

A4

forming a barrier metal layer and a copper layer within said dual damascene opening to complete said copper metallization in the fabrication of said integrated circuit device.

Please cancel Claim 13.

A5

17. (AMENDED) The method according to Claim 12 wherein said TEOS-based silicon oxide etch stop layer has a thickness of between about 50 and 5000 Angstroms.

Please cancel Claims 18-22.

Please add the following new Claims:

A6

23. The method according to Claim 12 wherein said TEOS-based silicon oxide capping layer has a thickness of between about 50 and 5000 Angstroms.

24. A method of forming a dielectric material layer comprising:

depositing a low dielectric constant material layer on a substrate wherein said low dielectric constant material comprises: porous or non-porous carbon-based silicon oxides, porous or non-porous doped silicon

oxides, porous or non-porous organic polymers, or porous or non-porous inorganic polymers;

implanting silicon ions into said low dielectric constant material layer to a depth of between about 50 and 600 Angstroms; and

thereafter depositing a TEOS-based silicon oxide layer overlying said low dielectric constant material whereby there is good adhesion between said low dielectric constant material layer and said TEOS-based silicon oxide layer.

25. The method according to Claim 24 wherein said low dielectric constant material layer has a thickness of between about 500 and 50,000 Angstroms.

26. The method according to Claim 24 wherein said step of implanting silicon ions into said low dielectric constant material layer comprises implanting said silicon ions at an energy of between about 5 and 30 KeV at a dosage of between about 1 E 12 and 1 E 16 ions/cm^2.

27. The method according to Claim 24 wherein said TEOS-based silicon oxide layer has a thickness of between about 50 and 5000 Angstroms.

28. A method of dual damascene copper metallization in the fabrication of an integrated circuit device comprising:

depositing a first low dielectric constant material layer over a substrate wherein said first low dielectric constant material comprises: porous or non-porous carbon-based silicon oxides, porous or non-porous doped silicon oxides, porous or non-porous organic polymers, or porous or non-porous inorganic polymers;

implanting silicon ions into said first low dielectric constant material layer to a depth of between about 50 and 600 Angstroms;

thereafter depositing a TEOS-based silicon oxide etch stop layer overlying said first low dielectric constant material whereby there is good adhesion between said first low dielectric constant material layer and said TEOS-based silicon oxide etch stop layer;

depositing a second low dielectric constant material layer overlying said etch stop layer wherein said second low dielectric constant material comprises: porous or non-porous carbon-based silicon oxides, porous or non-porous doped silicon oxides, porous or non-porous organic polymers, or porous or non-porous inorganic polymers;

implanting silicon ions into said second low

dielectric constant material layer to a depth of between about 50 and 600 Angstroms;

thereafter depositing a TEOS-based silicon oxide capping layer overlying said second low dielectric constant material whereby there is good adhesion between said second low dielectric constant material layer and said TEOS-based silicon oxide capping layer;

forming a dual damascene opening through said capping layer, said second low dielectric constant material layer, said etch stop layer, and said first low dielectric constant material layer; and

forming a barrier metal layer and a copper layer within said dual damascene opening to complete said copper metallization in the fabrication of said integrated circuit device.

29. The method according to Claim 28 wherein said first and second low dielectric constant material layers have a thickness of between about 500 and 50,000 Angstroms.

30. The method according to Claim 28 wherein said steps of implanting silicon ions into said first and second low dielectric constant material layers comprises implanting said silicon ions at an energy of between about 5 and 30 KeV at a dosage of between about 1 E 12